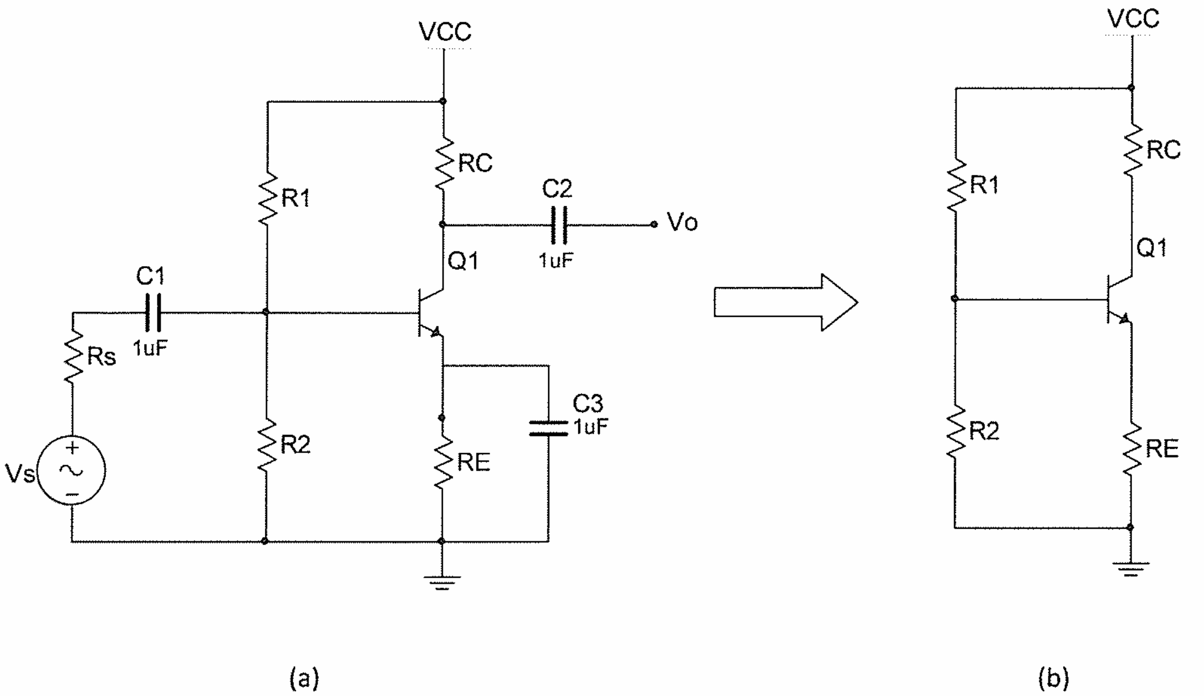
A.C Analysis of BJT Amplifiers

**For D.C analysis*

Open all the capacitors for example for the cct. Shown in Fig(1)



Fig(1) Transistor circuit under examination in D.C analysis

**for A.C analysis*

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent
3. Removing all elements bypassed by the short-circuit equivalents introduced

   by steps 1 and 2
4. Redrawing the network in a more convenient and logical form Fig(1a)

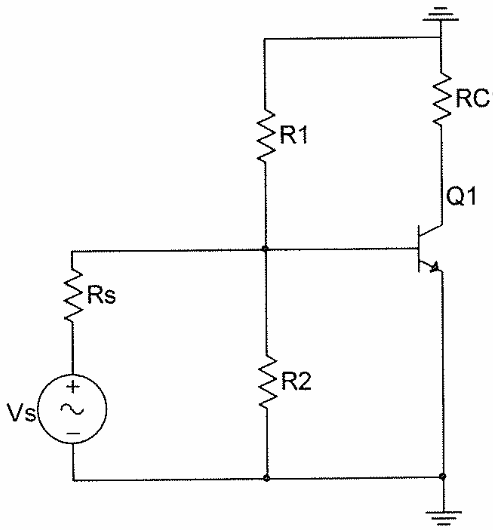


Figure (2) The network of Fig(1a) following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors

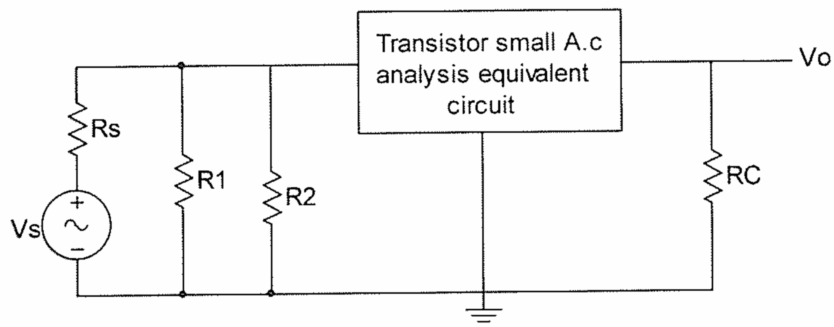


Figure 3 Circuit of Fig. 2redrawn for small-signal ac analysis

BJT transistor modelling

1. The Hybrid Equivalent Model (Complete Model)

hi = input resistor

hr = reveres transfer voltage ratio

hf = forward transfer current ratio

ho = output conductance

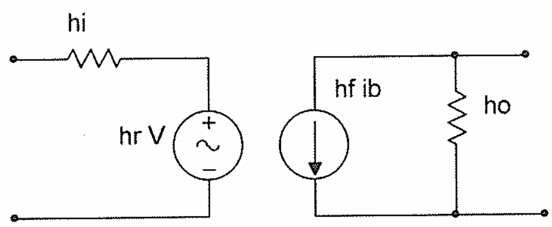


Fig.4 The Hybrid Equivalent Model

2. Approximate Equivalent Circuit

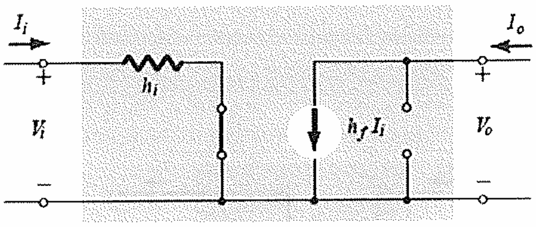


Figure 5a Effect of removing *hre* and *hoe* from the equivalent model

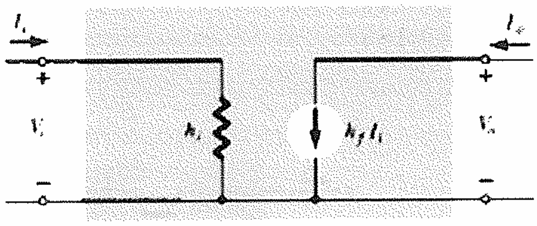


Figure 5b Approximate hybrid hybrid equivalent circuit.

3. The re Transistor Model

** Common base*

$$\boxed{r_e = \frac{26\ \text{mV}}{I_E}}$$

$$\boxed{Z_i = r_e}_{CB}$$

$$\boxed{Z_o \cong \infty\ \Omega}_{CB}$$

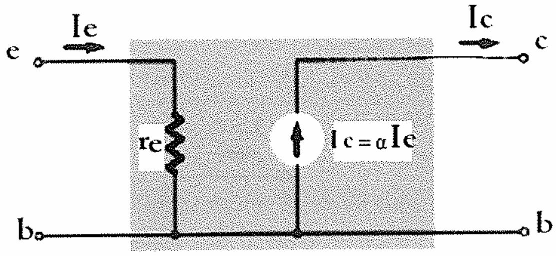


Fig.6 re-mode l

voltage gain will now be determined for the network of Fig. 2.14

$$V_o = -I_o R_L = -(-I_c) R_L = \alpha I_e R_L$$

$$V_i = I_e Z_i = I_e r_e$$

$$A_v = \frac{V_o}{V_i} = \frac{\alpha I_e R_L}{I_e r_e}$$

$$\boxed{A_v = \frac{\alpha R_L}{r_e} \cong \frac{R_L}{r_e}}_{CB}$$

$$A_i = \frac{I_o}{I_i} = \frac{-I_c}{I_e} = -\frac{\alpha I_e}{I_e}$$

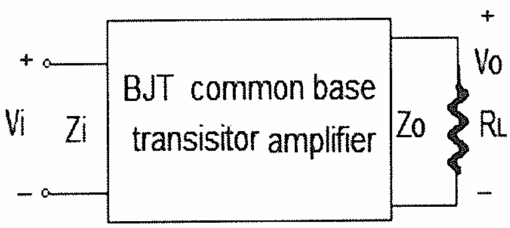


Figure 7 Defining *Av* for the common- base configuration

$$\boxed{A_i = -\alpha \cong -1}_{CB}$$

The approximation model for common base transistor shown in fig(2.15)

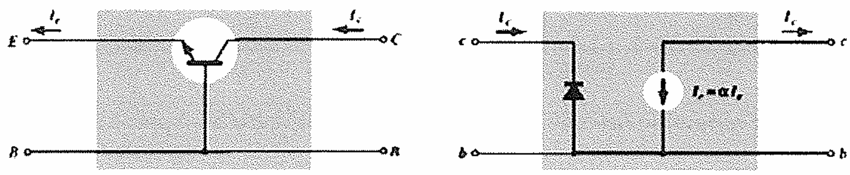


Figure 8 Approximate models for a common-base *npn* transistor configuration

*Common Emitter

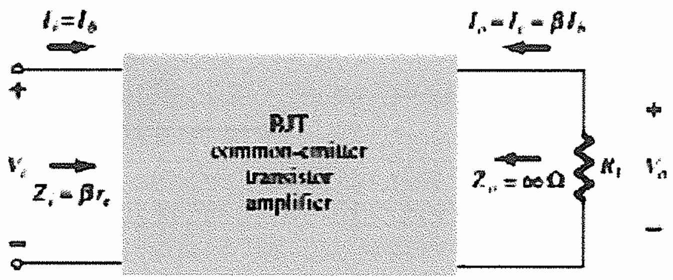


Figure 9 Determining the voltage and current gain for the common-emitter transistor amplifier.

$$V_o = -I_oR_L = -I_cR_L = -\beta I_bR_L$$

$$V_i = I_iZ_i = I_b\beta r_e$$

$$A_v = \frac{V_o}{V_i} = -\frac{\beta I_bR_L}{I_b\beta r_e}$$

$$\boxed{A_v = -\frac{R_L}{r_e}}_{CE, r_o = \infty\Omega}$$

The current gain for the configuration of Fig. 2.18

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$$

$$\boxed{A_i = \beta}\Big|_{CE, r_o = \infty\ \Omega}$$

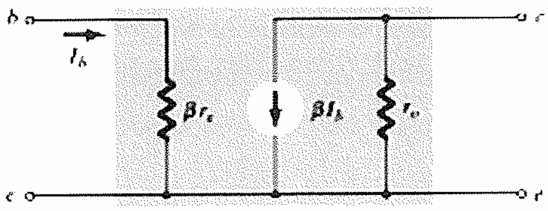


Figure 10 *re* model for the common-emitter transistor configuration

equivalent model *hybrid equivalent circuit.*

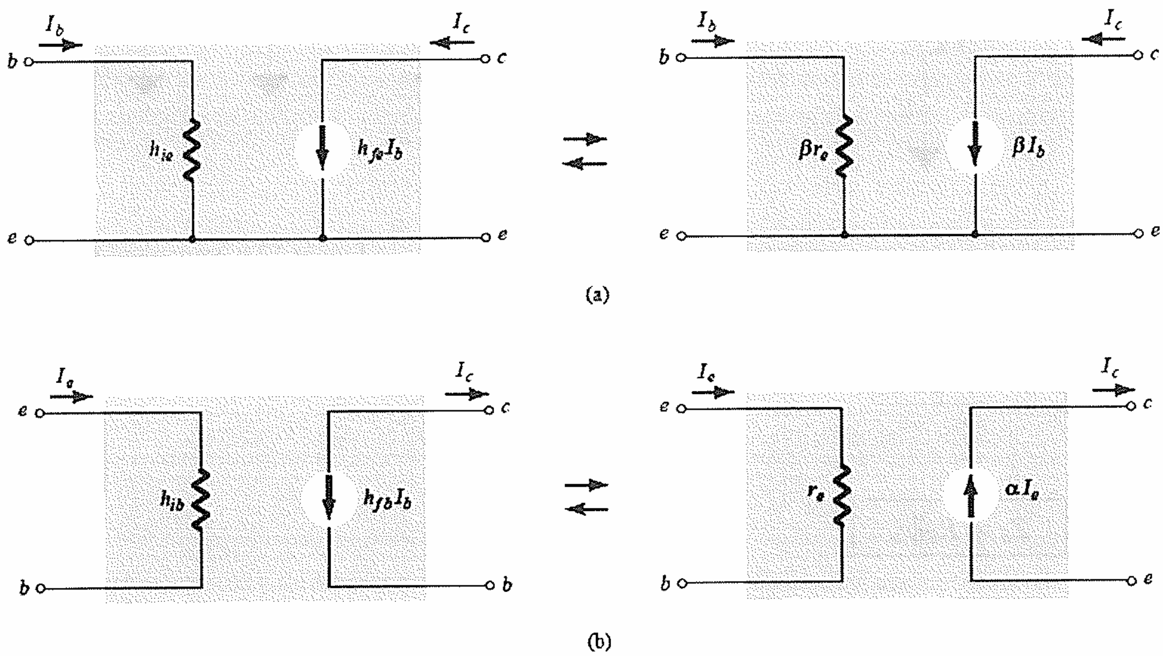


Figure 11 Hybrid versus *re* model: (a) common-emitter configuration;
(b) common-base configuration.

$h_{ie} = \beta r_e$, $h_{fe} = \beta$

$h_{ib} = r_e$, $h_{fb} = -\alpha$

BJT Small-Signal Analysis

1. Common-Emitter Amplifier Configuration

*Fixed-Bias

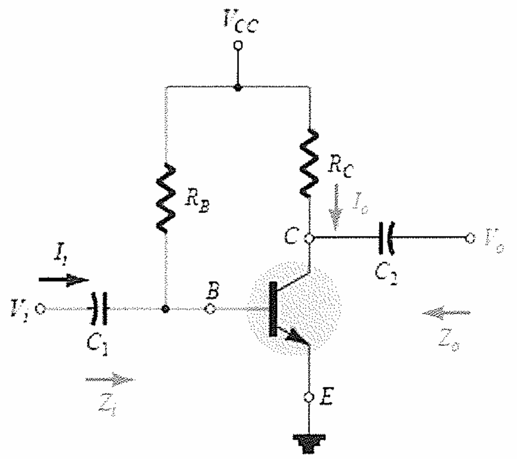


Figure 12.a Common-emitter fixed-bias

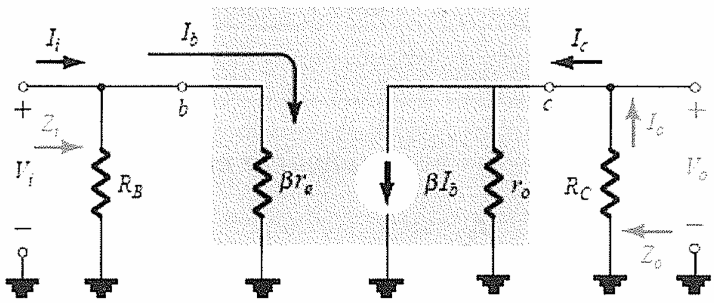


Figure 12.b equivalent circuit

$$\boxed{Z_i = R_B \| \beta r_e}$$

$$\boxed{Z_o = R_C \| r_o}$$

$$\boxed{Z_o \cong R_C}$$

If $r_o \geq 10\ R_D$, the approximation $R_C \| r_o \cong R_C$ is frequently applied and

$$\boxed{Z_i \cong \beta r_e}_{R_B \geq 10\beta r_e}$$

A_v: The resistors r_o and R_C are in parallel,

and $$V_o = -\beta I_b (R_C \| r_o)$$

but $$I_b = \frac{V_i}{\beta r_e}$$

so that $$V_o = -\beta\left(\frac{V_i}{\beta_{r_e}}\right)(R_C \| r_o)$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}}$$

If $r_o \geq 10R_C$,

$$\boxed{A_v = -\frac{R_C}{r_e}}_{r_o \geq 10R_C}$$

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}}$$

which is certainly an unwieldy, complex expression.

However, if $r_o \geq 10R_C$ and $R_B \geq 10\beta r_e$, which is often the case,

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R_B r_o}{(r_o)(R_B)}$$

and

$$\boxed{A_i \cong \beta}_{r_o \geq 10R_C,\ R_B \geq 10\beta r_e}$$

Phase Relationship: The negative sign in the resulting equation for *Av* reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 13.

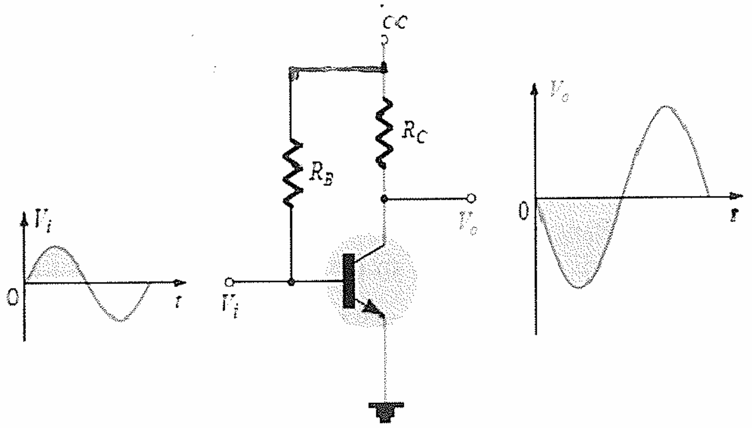


Figure (13) Demonstrating the 180° phase shift between inputs and output waveforms.

Example:1

For the network of Fig.(14):

(a) Determine r_e.
(b) Find Z_i (with $r_o = \infty\ \Omega$).
(c) Calculate Z_o (with $r_o = \infty\ \Omega$).
(d) Determine A_v (with $r_o = \infty\ \Omega$).
(e) Find A_i (with $r_o = \infty\ \Omega$).
(f) Repeat parts (c) through (e) including $r_o = 50\ \text{k}\Omega$ in all calculations and compare results.

Solution

(a) DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.428\ \text{mA}} = \mathbf{10.71\ \Omega}$$

(b) $\beta r_e = (100)(10.71\ \Omega) = 1.071\ \text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\ \text{k}\Omega \| 1.071\ \text{k}\Omega = \mathbf{1.069\ k\Omega}$$

(c) $Z_o = R_C = \mathbf{3\ k\Omega}$

(d) $A_v = -\dfrac{R_C}{r_e} = -\dfrac{3\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$

(e) Since $R_B \geq 10\beta r_e (470\ \text{k}\Omega > 10.71\ \text{k}\Omega)$

$$A_i \cong \beta = \mathbf{100}$$

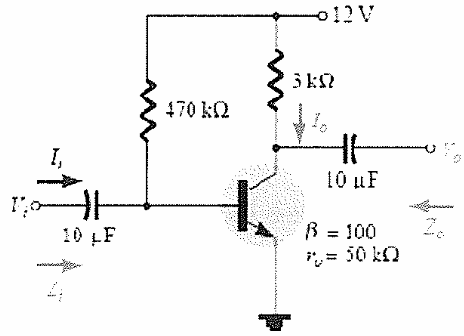


Figure 14.

(f) $Z_o = r_o \| R_C = 50\ \text{k}\Omega \| 3$ … $\mathbf{3\ k\Omega}$ vs. $3\ \text{k}\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-264.24} \text{ vs. } -280.11$$

$$A_i = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)} = \frac{(100)(470\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 3\ \text{k}\Omega)(470\ \text{k}\Omega + 1.071\ \text{k}\Omega)}$$

$$= \mathbf{94.13} \text{ vs. } 100$$

As a check:

$$A_i = -A_v \frac{Z_i}{R_C} = \frac{-(-264.24)(1.069\ \text{k}\Omega)}{3\ \text{k}\Omega} = \mathbf{94.16}$$

Example: 2

For the network of Fig. 15 determined:

(a) Z_i, (b) Z_o (c) A_V (d) A_I

(a) $Z_i = R_B \| h_{ie} = 330\ \text{k}\Omega \| 1.175\ \text{k}\Omega$

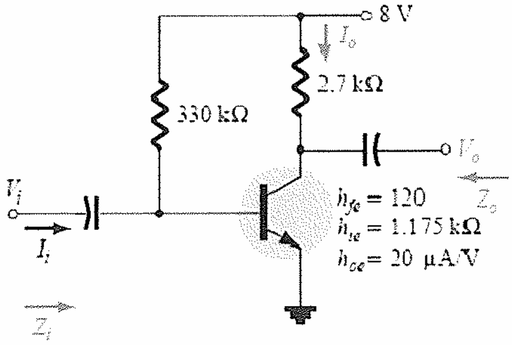
$\cong h_{ie} = \mathbf{1.171\ k\Omega}$

(b) $r_o = \dfrac{1}{h_{oe}} = \dfrac{1}{20\ \mu\text{A/V}} = 50\ \text{k}\Omega$

$Z_o = \dfrac{1}{h_{oe}} \| R_C = 50\ \text{k}\Omega \| 2.7\ \text{k}\Omega = \mathbf{2.56\ k\Omega} \cong R_C$

(c) $A_V = -\dfrac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} = -\dfrac{(120)(2.7\ \text{k}\Omega \| 50\ \text{k}\Omega)}{1.171\ \text{k}\Omega} =$

(d) $A_i \cong h_{fe} = 120$



Fig(15)

*Voltage-divider

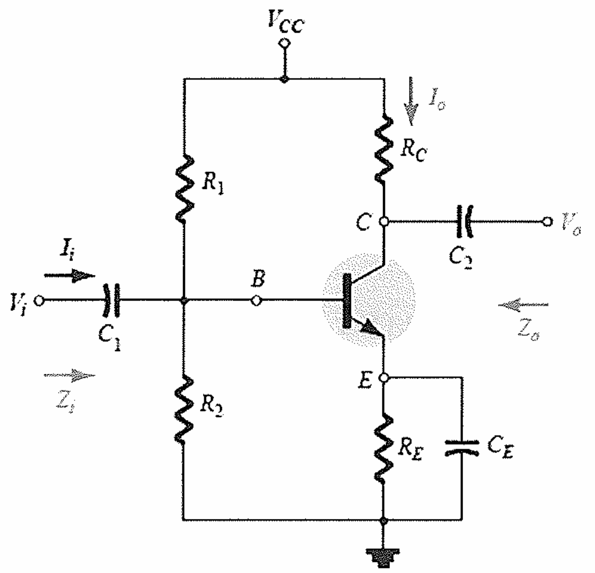


Figure 16.a Voltage-divider bias configurations.

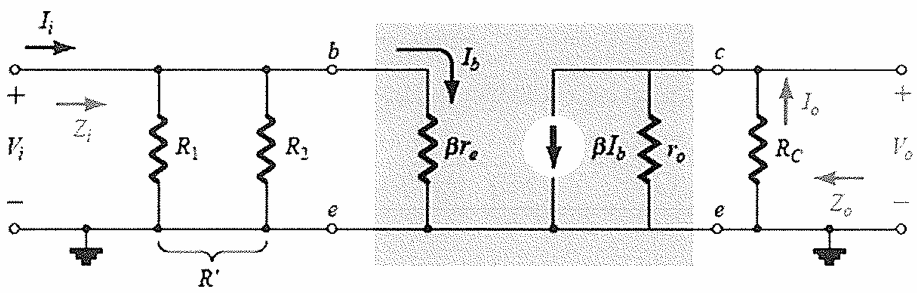


Figure 16.b Substituting the *re* equivalent circuit into the ac equivalent network of Fig. 16.b

$$\boxed{R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}}$$

$$\boxed{Z_i = R' \| \beta r_e}$$

$$\boxed{Z_o = R_C \| r_o}$$

If $r_o \geq 10R_C$,

$$\boxed{Z_o \cong R_C}_{r_o \geq 10R_C}$$

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}}$$

For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e}}_{r_o \geq 10R_C}$$

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)}}$$

For $r_o \geq 10R_C$,

$$\boxed{A_i = \frac{I_o}{I_i} \cong \frac{\beta R'}{R' + \beta r_e}}_{r_o \geq 10R_C}$$

And if $R' \geq 10\beta r_e$,

$$\boxed{A_i = \frac{I_o}{I_i} \cong \beta}_{r_o \geq 10R_C,\ R' \geq 10\beta r_e}$$

$$\boxed{A_i = -A_v \frac{Z_i}{R_C}}$$

Phase relationship: The negative sign of equation above reveals a 180° phase shift between *Vo* and *Vi*.

Example : 3

For the network of Fig. 17, determine

(a) r_e.
(b) Z_i.
(c) Z_o ($r_o = \infty\ \Omega$).
(d) A_v ($r_o = \infty\ \Omega$).
(e) A_i ($r_o = \infty\ \Omega$).
(f) The parameters of parts (b) through (e) if $r_o = 1/h_{oe} = 50\ \text{k}\Omega$ and compare results.

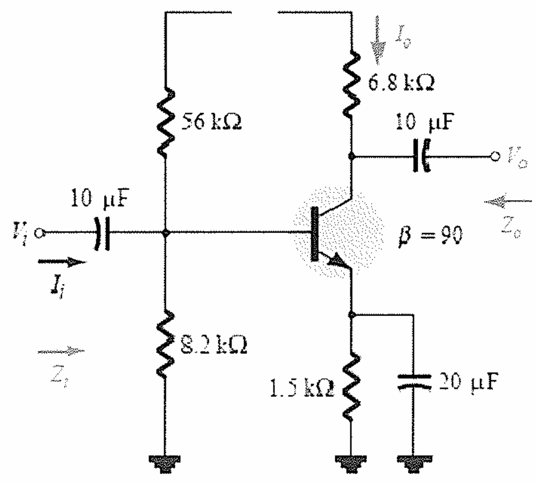


Figure 17 Example 3.

(a) DC: Testing $\beta R_E > 10R_2$

$$(90)(1.5\ \text{k}\Omega) > 10(8.2\ \text{k}\Omega)$$

$$135\ \text{k}\Omega > 82\ \text{k}\Omega\ (\textit{satisfied})$$

Using the approximate approach,

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\ \text{k}\Omega)(22\ \text{V})}{56\ \text{k}\Omega + 8.2\ \text{k}\Omega} = 2.81\ \text{V}$$

$$V_E = V_B - V_{BE} = 2.81\ \text{V} - 0.7\ \text{V} = 2.11\ \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11\ \text{V}}{1.5\ \text{k}\Omega} = 1.41\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.41\ \text{mA}} = \mathbf{18.44\ \Omega}$$

(b) $R' = R_1 \| R_2 = (56\ \text{k}\Omega) \| (8.2\ \text{k}\Omega) = 7.15\ \text{k}\Omega$

$Z_i = R' \| \beta r_e = 7.15\ \text{k}\Omega \| (90)(18.44\ \Omega) = 7.15\ \text{k}\Omega \| 1.66\ \text{k}\Omega$

$= \mathbf{1.35\ k\Omega}$

(c) $Z_o = R_C = \mathbf{6.8\ k\Omega}$

(d) $A_v = -\dfrac{R_C}{r_e} = -\dfrac{6.8\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

(e) The condition $R' \geq 10\beta r_e$ $(7.15\ \text{k}\Omega \geq 10(1.66\ \text{k}\Omega) = 16.6\ \text{k}\Omega$ is *not* satisfied. Therefore,

$$A_i \cong \frac{\beta R'}{R' + \beta r_e} = \frac{(90)(7.15\ \text{k}\Omega)}{7.15\ \text{k}\Omega + 1.66\ \text{k}\Omega} = \mathbf{73.04}$$

(f) $Z_i = \mathbf{1.35\ k\Omega}$

$$Z_o = R_C \| r_o = 6.8\ \text{k}\Omega \| 50\ \text{k}\Omega = \mathbf{5.98\ k\Omega} \text{ vs. } 6.8\ \text{k}\Omega$$

$$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-324.3} \text{ vs. } -368.76$$

The condition

$$r_o \geq 10R_C \ (50\ \text{k}\Omega \geq 10(6.8\ \text{k}\Omega) = 68\ \text{k}\Omega)$$

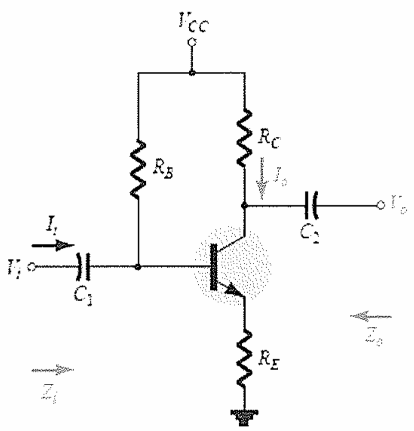
is *not* satisfied. Therefore,

$$A_i = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)} = \frac{(90)(7.15\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 6.8\ \text{k}\Omega)(7.15\ \text{k}\Omega + 1.66\ \text{k}\Omega)}$$
$$= \mathbf{64.3} \text{ vs. } 73.04$$

There was a measurable difference in the results for Z_o, A_v, and A_i because the condition $r_o \geq 10R_C$ was *not* satisfied.

**Unbypassed configuration*

$$V_i = I_b \beta r_e + I_e R_E$$
$$V_i = I_b \beta r_e + (\beta + 1) I_b R_E$$



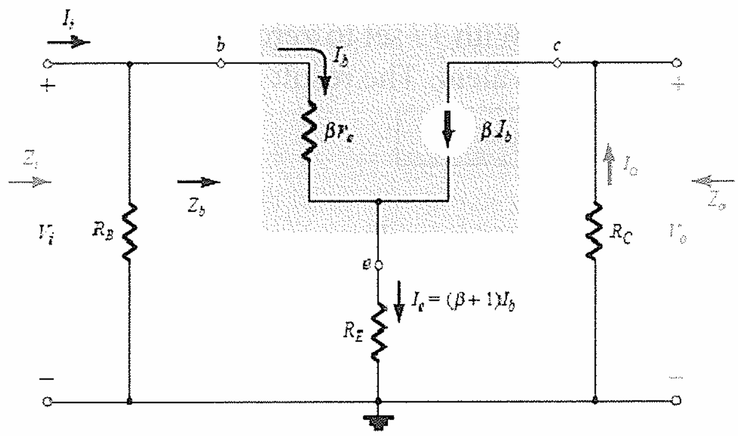


Figure 18.a CE emitter-bias configuration. Figure 18.b Substituting the *re* equivalent circuit

and the input impedance looking into the network to the right of R_b *is*

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E}$$

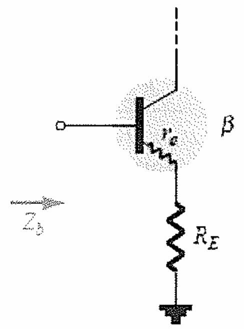


Figure 19 unbypassed emitter resistor.

$$Z_b \cong \beta r_e + \beta R_E$$

$$\boxed{Z_b \cong \beta(r_e + R_E)}$$

$$\boxed{Z_b \cong \beta(r_e + R_E)}$$

Since R_E is often much greater than re, Eq. Above can be further reduced to

$$\boxed{Z_b \cong \beta R_E}$$

From fig 2.33 we can determined Z_i

$$\boxed{Z_i = R_B \| Z_b}$$

Zo: With Vi set to zero, I_B= 0 and βI_B can be replaced by an open-circuit equivalent. The result is

$$\boxed{Z_o = R_C}$$

$$I_b = \frac{V_i}{Z_b}$$

$$V_o = -I_o R_C = -\beta I_b R_C$$

$$= -\beta\left(\frac{V_i}{Z_b}\right) R_C$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}}$$

Substituting $Z_b = \beta(r_e + R_E)$ gives

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E}}$$

and for the approximation $Z_b \cong \beta R_E$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E}$$

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B}{R_B + Z_b}$$

$$A_i = -A_v \frac{Z_i}{R_C}$$

Phase relationship: The negative sign in Equation above reveals a 180° phase shift between Vo and Vi.

2. Common-Base Amplifier Configuration

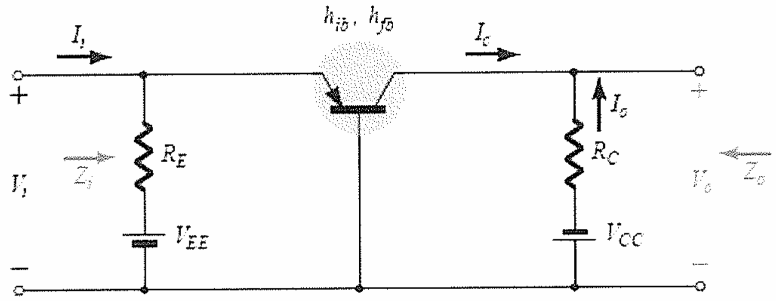


Figure 20.a Common-base configuration.

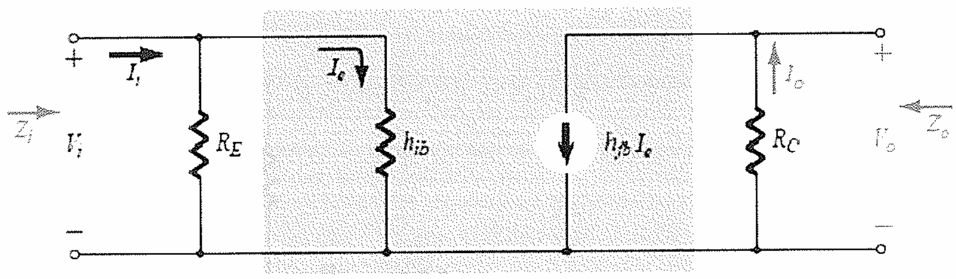


Figure 2.36 Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 20.b

Example

For the network of Fig. 21, determine:

(a) Z_i.
(b) Z_o.
(c) A_v.
(d) A_i.

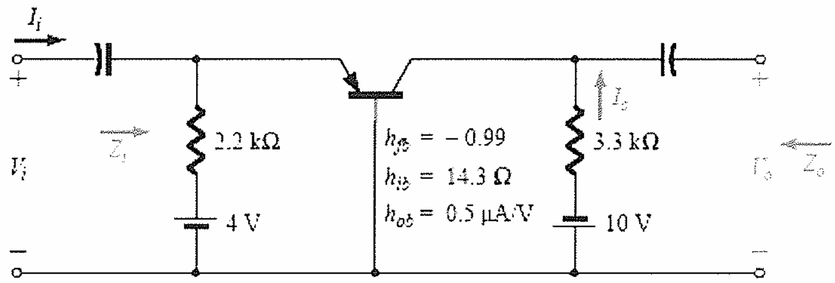


Fig.(21) Common base circuit

(a) $Z_i = R_E \| h_{ib} = 2.2\ \text{k}\Omega \| 14.3\ \Omega = \mathbf{14.21\ \Omega} \cong h_{ib}$

(b) $r_o = \dfrac{1}{h_{ob}} = \dfrac{1}{0.5\ \mu\text{A/V}} = 2\ \text{M}\Omega$

$$Z_o = \frac{1}{h_{ob}} \| R_C \cong R_C = \mathbf{3.3\ k\Omega}$$

(c) $A_v = -\dfrac{h_{fb} R_C}{h_{ib}} = -\dfrac{(-0.99)(3.3\ \text{k}\Omega)}{14.21} = \mathbf{229.91}$

(d) $A_i \cong h_{fb} = \mathbf{-1}$

3. *Common Collector Amplifier (Emitter Follower)*

Main Characteristics of C.C. Amplifier

1. Av< 1
2. High R_i
3. Low R_o
4. Phase shift = zero

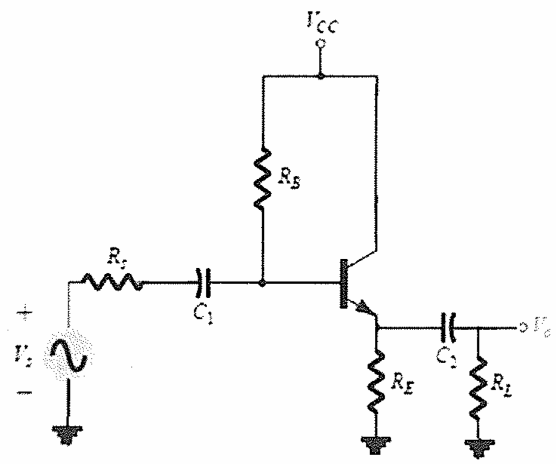


Fig.(22.a) Common collector circuit

Ac. Analysis of common collector with R_E

$$i_e = (1 + h_{fe})i_b$$

$$\boldsymbol{R_i = [(R_E \parallel R_L)(1 + h_{fe}) + h_{ie}] \parallel R_B}$$

$$\boldsymbol{R_o = \{\frac{[(R_s \parallel R_B) + h_{ie}]}{1 + h_{fe}}\} \parallel R_E}$$

$$A_v = \frac{V_o}{V_i}$$

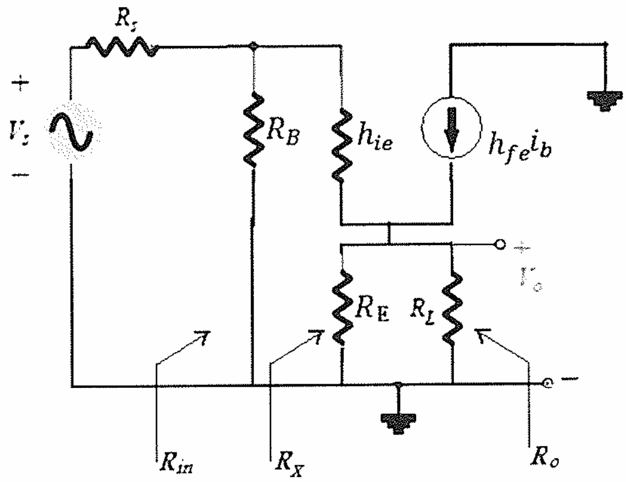


Fig.(22.b)
Equivalent circuit of common collector

$$\boldsymbol{Av = \frac{i_b(1 + h_{fe})(R_E \parallel R_L)}{i_b[h_{ie} + (1 + h_{fe})(R_E \parallel R_L)}}$$ $$A_v < 1$$

$$A_{IS} = \frac{I_o}{I_i} = \frac{I_o}{I_b} * \frac{I_b}{I_i}$$

$$\boldsymbol{= \frac{(1 + h_{fe})R_E}{R_E + R_L} * \frac{R_B}{R_B + R_x}}$$

$$\boldsymbol{R_x = h_{ie} + (1 + h_{fe})(R_E//R_L)}$$

H.w For the network of Fig. (23)*re =28Ω and β=200*

(a) Determine *Zi* and *Zo*.
(b) Find *Av* and *Ai*.
(c) Draw Vo with input voltage Vi = 100 sin(wt). mV

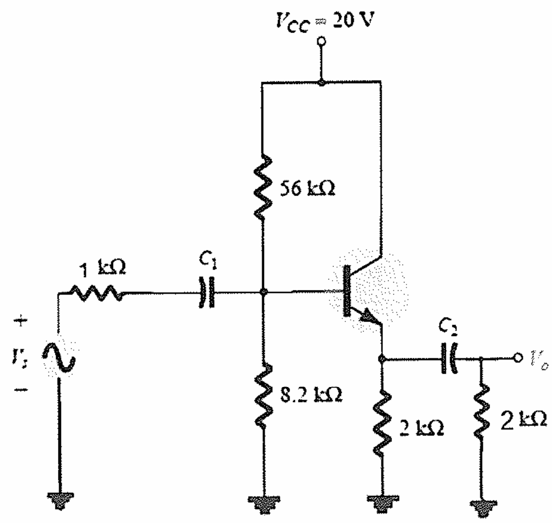
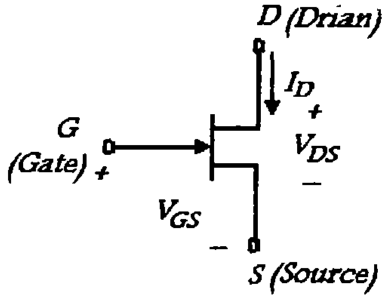


Fig. (23)

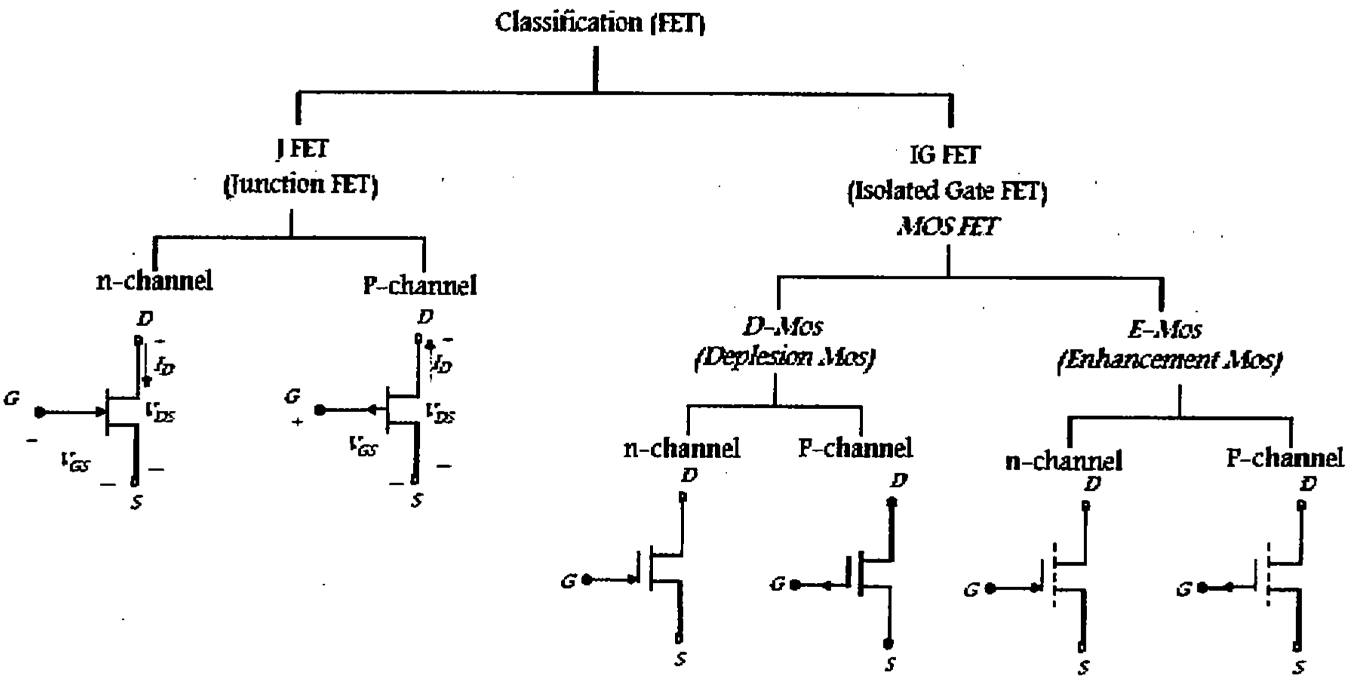
Field Effect Transistor (FET)

Main Characteristics

- It is unipolar device
- It has a very high input impedance
- It is a voltage controlled current source (VCCS)
- Small size and widely used in I.C fabrication
- Low noise
- Low voltage gain



Fig(1) FET

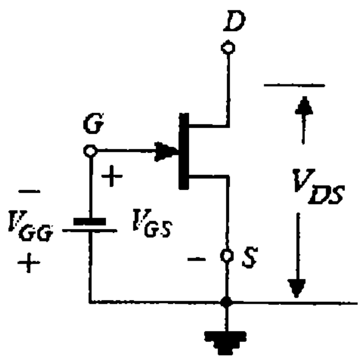


The main different between JFET & MOSFET are:

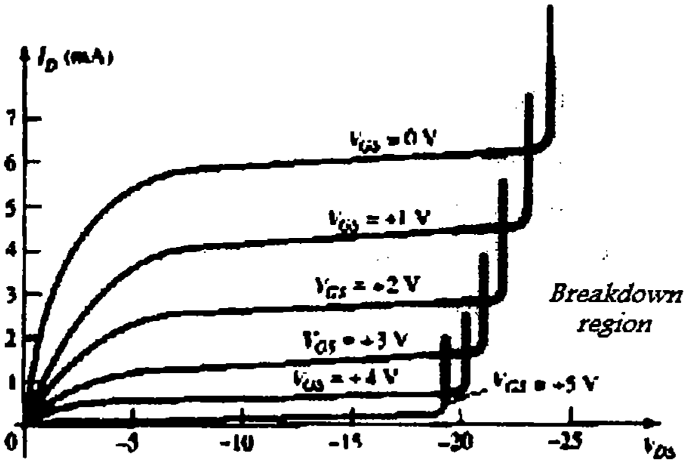
1. The MOSFET has an isolated liar between gate and drian and source therefore it has a very high input resistance compared to JFET
2. The MOSFET is very sensitive and effected by the static charge compared to the JFET which is rigid

Characteristics of JFET

Drian C/Cs (output C/Cs)



Fig(2a) JFET circuit



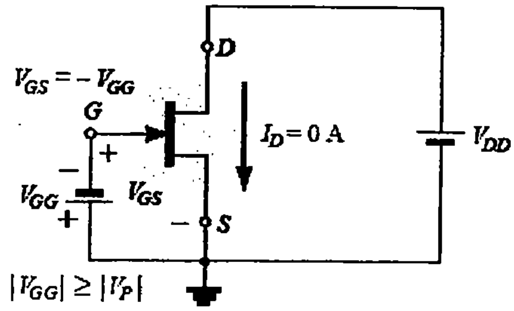
Fig(2b)c/cs of JFET

I_{DSS}=Drian source saturation current

V_p=Pinch-off voltage is negative voltage for n-channel devices and a positive voltage for p-channel JFETs

For active region operation G-S and D-S Jun must be reverse

$$I_D = F(V_{GS}) for\ a\ certian\ values\ of\ V_{GS}$$



Fig(3)

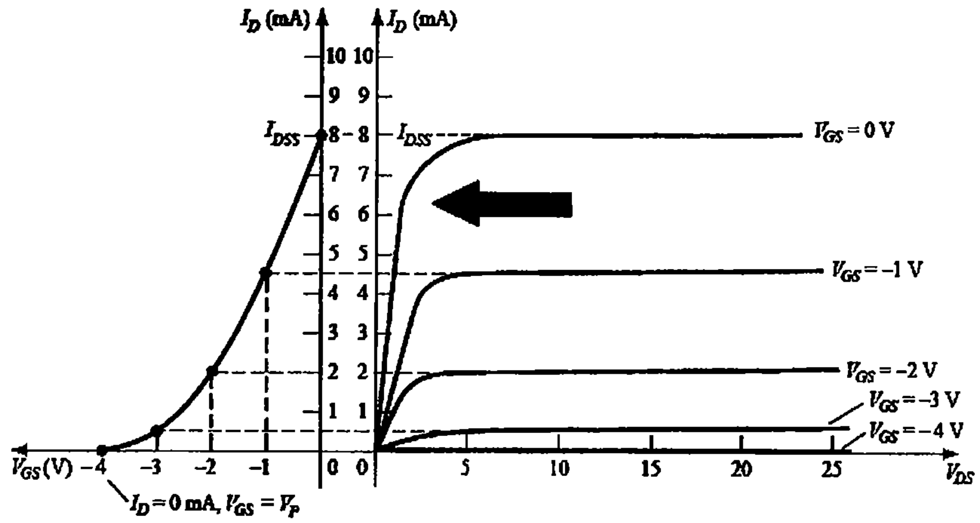
Transfer C/Cs

$I_D = F(V_{GS})$ and is given by Shockley's equation which is define by:

control variable

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

constants



Fig(4) The transfer C/Cs of JFET

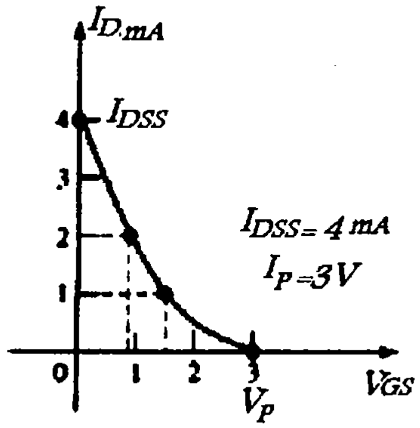
The transfer C/Cs can be draw when I_{DSS} *and* V_P are given

$V_{GS}(V)$	$I_D(mA)$
0	I_{DSS}
V_P	0
$\frac{1}{2}V_P$	$\frac{1}{4}I_{DSS}$
$\frac{1}{3}V_P$	$\frac{1}{2}I_{DSS}$

Example

Sketch the transfer curve for a *p*-channel device with I_{DSS} = 4 mA and V_P = 3 V.

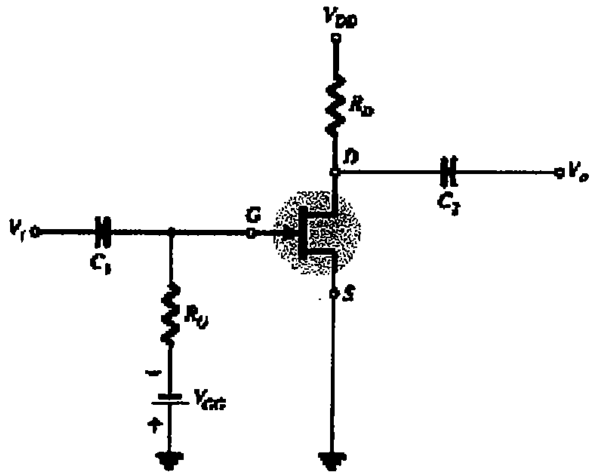
$V_{GS}(V)$	0	3	1.5	1
$I_D(mA)$	4	0	1	2



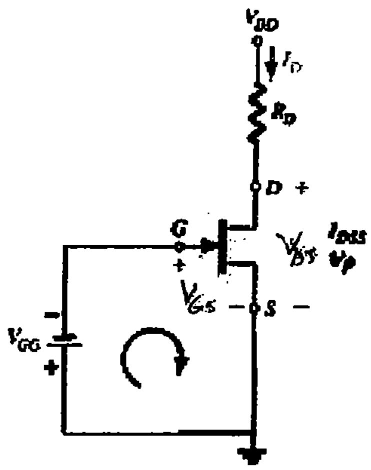
Fig(5) The transfer C/Cs

FET Biasing

- *FIXED-BIAS CONFIGURATION*



Fig(6a) Fixed bias of JFET



Fig(6b) dc analysis of JFET

$$V_{GS} = -V_{GG} \quad , \qquad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$V_{DS} = V_{DD} - I_D R_D$

$V_S = 0\text{ V}$

$V_{DS} = V_D - V_S$

$V_D = V_{DS} + V_S = V_{DS} + 0\text{ V}$

$V_D = V_{DS}$

$V_{GS} = V_G - V_S$

$V_G = V_{GS} + V_S = V_{GS} + 0\text{ V}$

$V_G = V_{GS}$

Example

Determine the following for the network of fig (7)

(a) V_{GSQ} (b)I_{DQ} (c)V_{DS}

(d)V_D (e)V_G (f)V_S

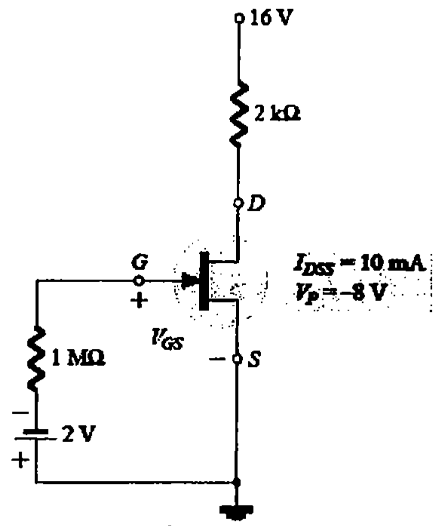


Fig (7)

Mathematical Approach:

(a) $V_{GS_Q} = -V_{GG} = \mathbf{-2\text{ V}}$

(b) $I_{D_Q} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \dfrac{-2\text{ V}}{-8\text{ V}}\right)^2$

$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$

$= \mathbf{5.625\text{ mA}}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$

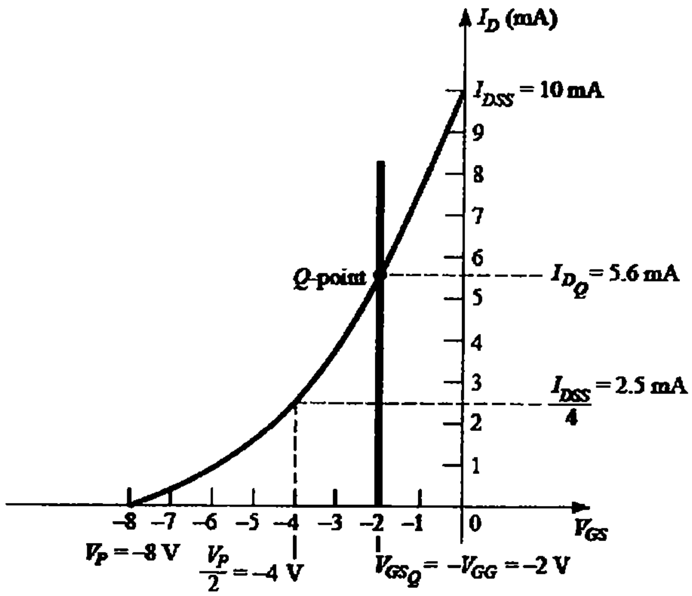
$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\text{ V}}$

(d) $V_D = V_{DS} = \mathbf{4.75\text{ V}}$

(e) $V_G = V_{GS} = \mathbf{-2\text{ V}}$

(f) $V_S = \mathbf{0\text{ V}}$

Graphical Approach



Fig(8) Graphically solution

$$V_{GS_Q} = -V_{GG} = -2\text{ V}$$

(b) $I_{D_Q} = \mathbf{5.6\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.6\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.2\text{ V} = \mathbf{4.8\ V}$

(d) $V_D = V_{DS} = 4.8\text{ V}$

(e) $V_G = V_{GS} = -2\text{ V}$

(f) $V_S = 0\text{ V}$

- *SELF-BIAS CONFIGURATION*

The controlling gate-to-source voltage is now determined by the voltage across a resistor Rs introduced in the source leg of the configuration

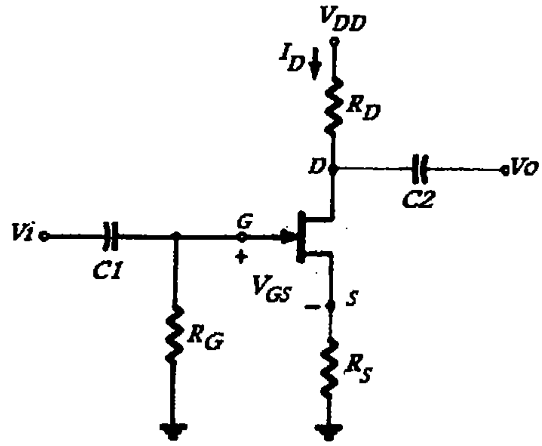


Fig (9) self bias

For the dc analysis, the capacitors can again be replaced by "open circuits

$$-V_{GS} - V_{R_S} = 0$$

$$V_{GS} = -V_{R_S}$$

$$\boxed{V_{GS} = -I_D R_S}$$

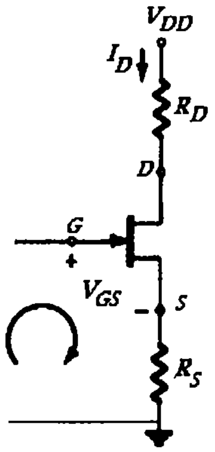


Fig (10) dc analysis of self bias

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

$$I_D = I_S$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)}$$

$$\boxed{V_S = I_D R_S}$$

$$\boxed{V_G = 0\ \text{V}}$$

$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}}$$

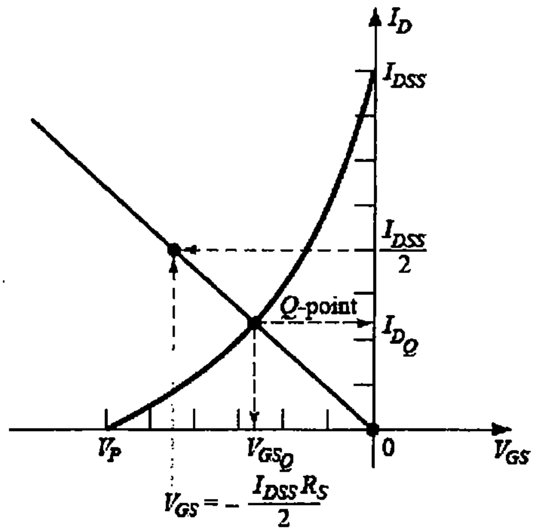


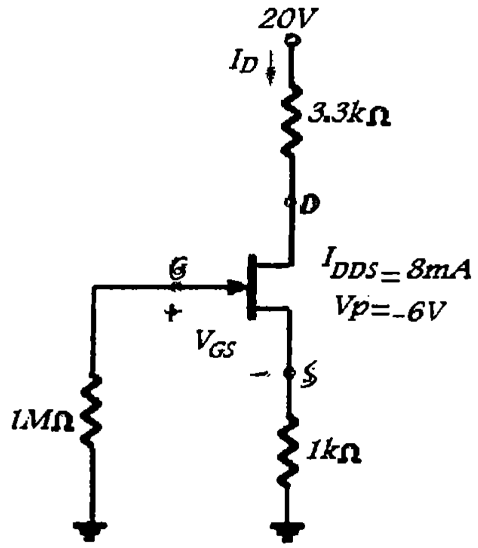
Fig (11) D.L.L

Example

Determine the following for the network of Fig. (12)

$(a) V_{GSQ}$ $(b) I_{DQ}$ $(c) V_{DS}$

$(d) V_S$ $(e) V_G$ $(f) V_D$



(a) The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4$ mA, we obtain

$$V_{GS} = -(4 \text{ mA})(1 \text{ k}\Omega) = -4 \text{ V}$$

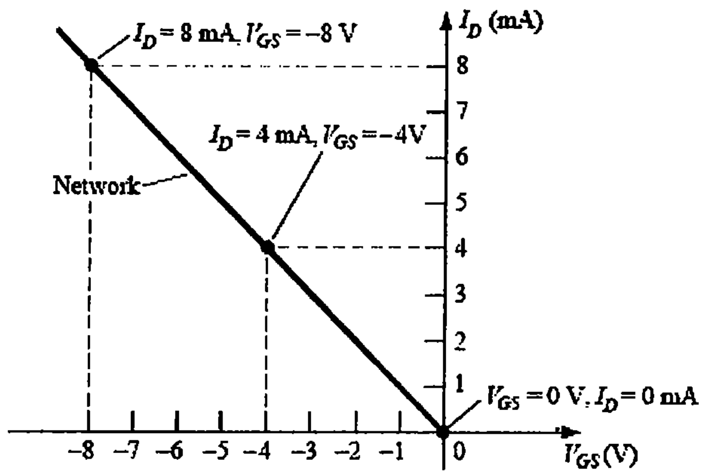


Figure 13 Sketching the selfbias line for the network of Fig12.

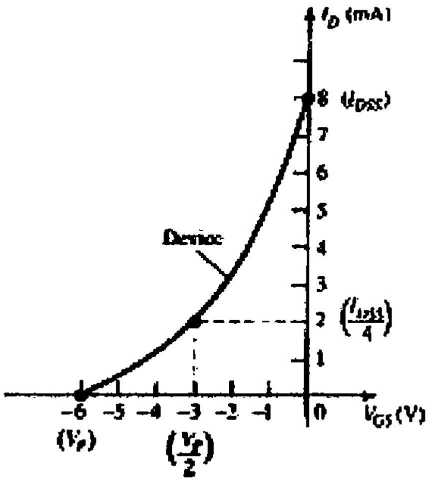


Figure.14 Sketching the device characteristics the for the JFET of Fig. 12.

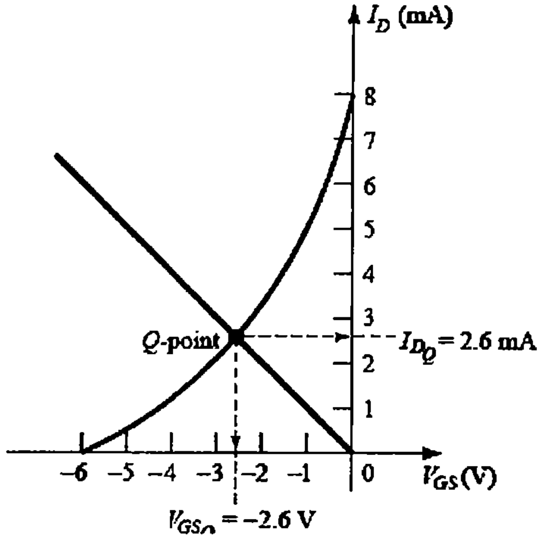


Figure 15 Determining the Q-point for network of Fig. 12.

(b) At the quiescent point:

$$I_{D_Q} = 2.6 \text{ mA}$$

(c) $V_{DS} = V_{DD} - I_D(R_S + R_D)$

$= 20 \text{ V} - (2.6 \text{ mA})(1 \text{ k}\Omega + 3.3 \text{ k}\Omega)$

$= 20 \text{ V} - 11.18 \text{ V}$

$= \mathbf{8.82 \text{ V}}$

(d) $V_S = I_D R_S$

$= (2.6 \text{ mA})(1 \text{ k}\Omega)$

$= \mathbf{2.6 \text{ V}}$

(e) $V_G = \mathbf{0 \text{ V}}$

(f) $V_D = V_{DS} + V_S = 8.82 \text{ V} + 2.6 \text{ V} = \mathbf{11.42 \text{ V}}$

or $V_D = V_{DD} - I_D R_D = 20 \text{ V} - (2.6 \text{ mA})(3.3 \text{ k}\Omega) = \mathbf{11.42 \text{ V}}$

Voltage-Divider Biasing

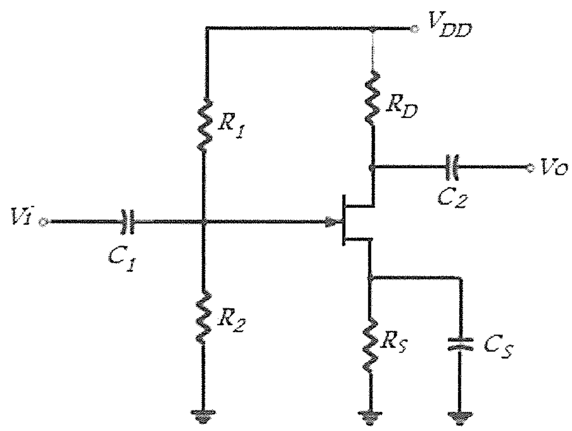
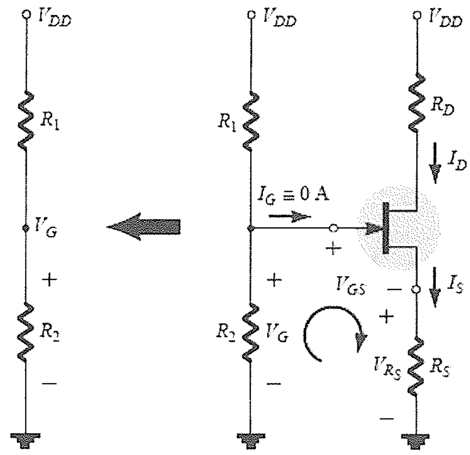


Fig (1a) Voltage dvider bias arrangement



Redrawn network of fig (1b) for dc analysis

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig (1.b) will result in

$$V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

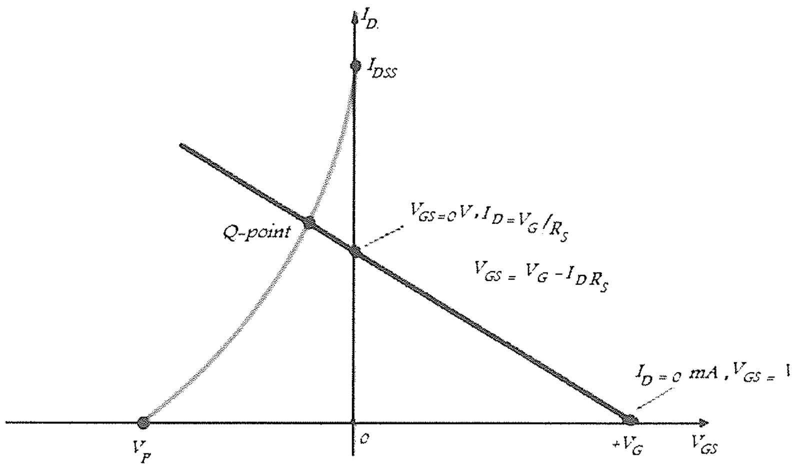
$$V_{GS} = V_G - I_D R_S$$

To draw c/cs

$$V_{GS} = V_G \big|_{I_D = 0\ \text{mA}}$$

$$V_{GS} = V_G - I_D R_S$$

$$0\ \text{V} = V_G - I_D R_S$$



Fig(2) trans. c/cs

$$I_D = \left.\frac{V_G}{R_S}\right|_{V_{GS} = 0\text{ V}}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

Example

Determine the following for the network of Fig(3).

(a) I_{D_Q} and V_{GS_Q}.
(b) V_D.
(c) V_S.
(d) V_{DS}.
(e) V_{DG}.

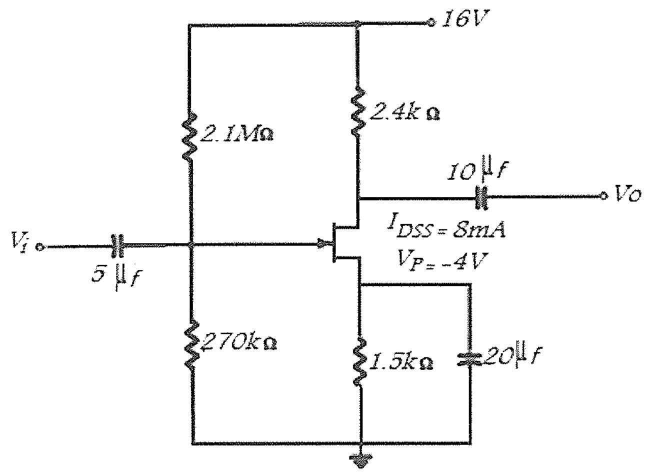
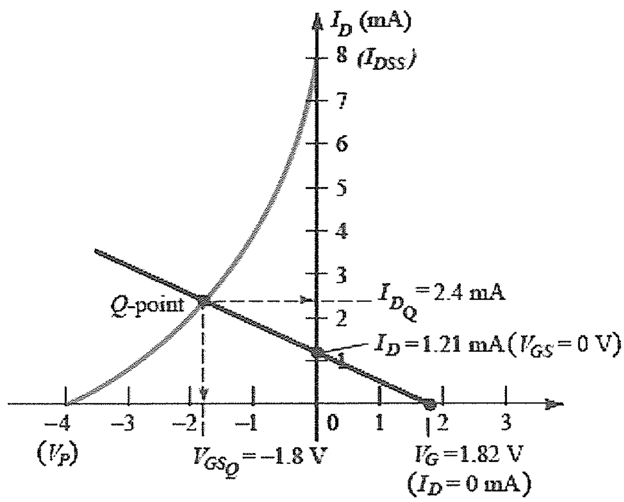


Fig (3) Voltage dvider circuit

(a) for the transfer c/cs if $I_D = \frac{I_{DSS}}{4} =$ $8mA/4$ =2mA ,

$$V_{GS} = \frac{V_P}{2} = -\frac{4V}{2} = -2$$

The resulting curve representing Shockley's equation fig (4), then



Fig(4)

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$
$$= \frac{(270\ \text{k}\Omega)(16\ \text{V})}{2.1\ \text{M}\Omega + 0.27\ \text{M}\Omega}$$
$$= 1.82\ \text{V}$$

$$V_{GS} = V_G - I_D R_S$$
$$= 1.82\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

When $I_D = 0$ mA:

$$V_{GS} = +1.82\ \text{V}$$

When $V_{GS} = 0$ V:

$$I_D = \frac{1.82\ \text{V}}{1.5\ \text{k}\Omega} = 1.21\ \text{mA}$$

The resulting bias line appears on Fig. 4 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\ mA}$$
$$V_{GS_Q} = \mathbf{-1.8\ V}$$

(b) $V_D = V_{DD} - I_D R_D$
$= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega)$
$= \mathbf{10.24\ V}$

(c) $V_S = I_D R_S = (2.4\ \text{mA})(1.5\ \text{k}\Omega)$
$= \mathbf{3.6\ V}$

(d) $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega + 1.5\ \text{k}\Omega)$
$= \mathbf{6.64\ V}$
or $V_{DS} = V_D - V_S = 10.24\ \text{V} - 3.6\ \text{V}$
$= \mathbf{6.64\ V}$

$$V_{DG} = V_D - V_G$$
$$= 10.24\ \text{V} - 1.82\ \text{V}$$
$$= \mathbf{8.42\ V}$$

<u>***Common Gate***</u>

Example

Determine the following for the common-gate configuration of Fig. 6.17.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_D.
(d) V_G.
(e) V_S.
(f) V_{DS}.

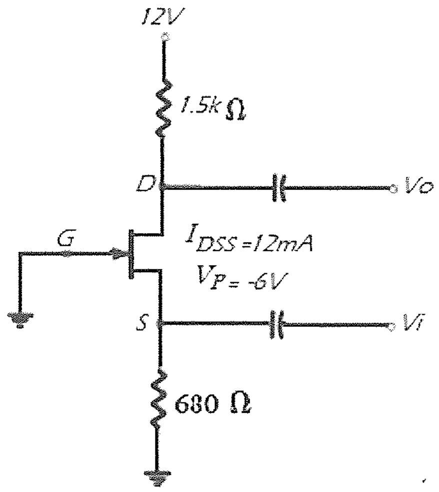


Fig (5a) Common gate circuit

(a) The transfer characteristics and load line appear in Fig. 6.19. In this case, the second point for the sketch of the load line was determined by choosing (arbitrarily) I_D= 6 mA and solving forV_{GS}. That is,

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA} \quad , \qquad V_{GS} = \frac{V_P}{2} = -\frac{6\text{ V}}{2} = -3\text{ V}$$

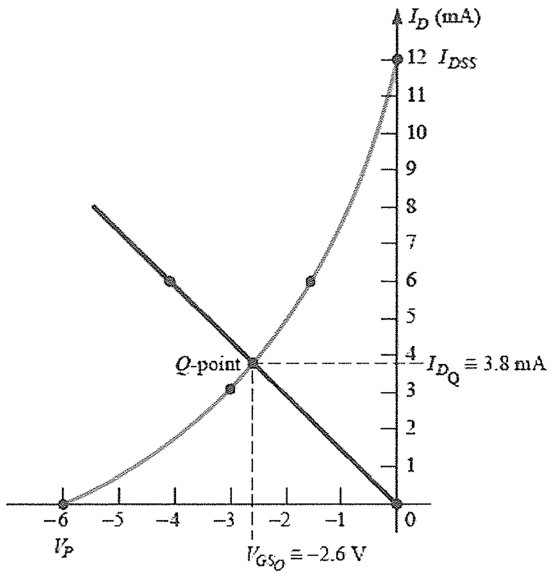


Figure 6 Determining the Q-point for the network of Fig.(5a)

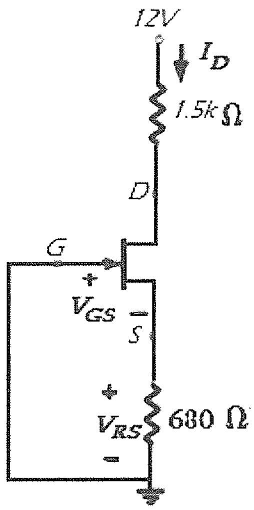


Figure (5b) Sketching the dc equivale the network of Fig. 5

as shown on Fig. 6Using the resulting quiescent point of Fig. 6 results in

(b)

$$V_{GS_Q} \cong -2.6\ \mathbf{V}$$

$$I_{D_Q} \cong 3.8\ \mathbf{mA}$$

(c) $V_D = V_{DD} - I_D R_D$
$= 12\ \text{V} - (3.8\ \text{mA})(1.5\ \text{k}\Omega) = 12\ \text{V} - 5.7\ \text{V}$
$= \mathbf{6.3\ V}$

(d) $V_G = \mathbf{0\ V}$

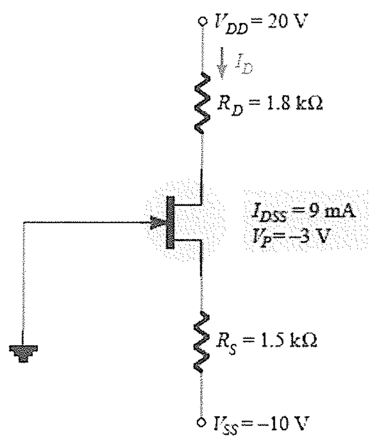
(e) $V_S = I_D R_S = (3.8\ \text{mA})(680\ \Omega)$
$= \mathbf{2.58\ V}$

(f) $V_{DS} = V_D - V_S$
$= 6.3\ \text{V} - 2.58\ \text{V}$
$= \mathbf{3.72\ V}$

Example

Determine the following for the network of fig (7a)

(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS}.
(c) V_D.
(d) V_S.



Fig(7a)

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

$$V_{GS} = V_{SS} - I_S R_S$$

$$I_S = I_D$$

$$\boxed{V_{GS} = V_{SS} - I_D R_S}$$

$$V_{GS} = 10\text{ V} - I_D(1.5\text{ k}\Omega)$$

For $I_D = 0$ mA,

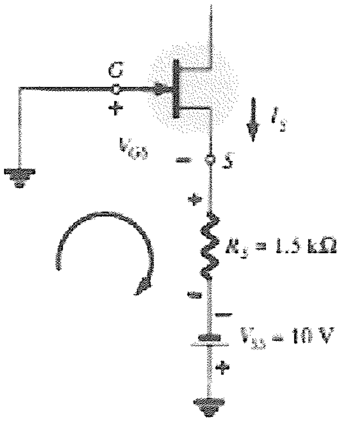
$$V_{GS} = V_{SS} = 10\text{ V}$$

For $V_{GS} = 0$ V,

$$0 = 10\text{ V} - I_D(1.5\text{ k}\Omega)$$

and

$$I_D = \frac{10\text{ V}}{1.5\text{ k}\Omega} = 6.67\text{ mA}$$



Fig(7b) Determining the network equation for the configuration of Fig7a

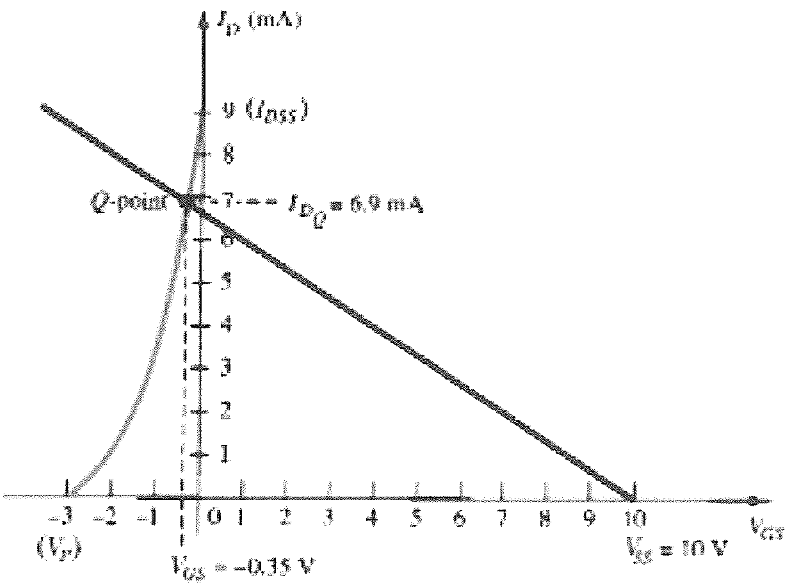


Figure 8 Determining the Q-point for the network of Fig 7a

The transfer characteristics are sketched using the plot point established by $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5$ V and $I_D = I_{DSS}/4 = 9\text{ mA}/4 = 2.25$ mA, as also appearing on Fig.8.The resulting operating point establishes the following quiescent levels:

$$I_{D_Q} = 6.9\text{ mA}$$

$$V_{GS_Q} = -0.35\text{ V}$$

(b) Applying Kirchhoff's voltage law to the output side of Fig. 7a will result in

$$-V_{SS} + I_S R_S + V_{DS} + I_D R_D - V_{DD} = 0$$

Substituting $I_S = I_D$ and rearranging gives

$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)}$$

which for this example results in

$$\begin{aligned} V_{DS} &= 20\text{ V} + 10\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega + 1.5\text{ k}\Omega) \\ &= 30\text{ V} - 22.77\text{ V} \\ &= \mathbf{7.23\ V} \end{aligned}$$

(c) $$\begin{aligned} V_D &= V_{DD} - I_D R_D \\ &= 20\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega) = 20\text{ V} - 12.42\text{ V} \\ &= \mathbf{7.58\ V} \end{aligned}$$

(d) $V_{DS} = V_D - V_S$

or $$\begin{aligned} V_S &= V_D - V_{DS} \\ &= 7.58\text{ V} - 7.23\text{ V} \\ &= \mathbf{0.35\ V} \end{aligned}$$